In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1-10. (Canceled)

11. (New) A method of compressing a timing trace stream which has a logic signal associated with each clock cycle of a target device, comprising:

determining that, during an instance of a preselected number of consecutive clock cycles, at least one logic signal at a first logic level and at least one logic signal at a second logic level are associated with respective ones of said clock cycles, and thereafter transmitting a first number of packets containing logic signals respectively associated with the preselected number of clock cycles; and

determining that, during a further instance of said preselected number of consecutive clock cycles, the logic signals associated with the respective clock cycles all have a same logic level, and thereafter, instead of transmitting a corresponding said first number of packets, transmitting a compressed representation of the corresponding said first number of packets, wherein said compressed representation is formatted within a second number of said packets and contains an indication of said same logic level and an indication of said preselected number, and wherein said second number of packets is less than said first number of packets.

12. (New) The method of Claim 11, wherein one of said logic levels indicates activity of a program counter during the corresponding clock cycle, and the other of said logic levels

indicates inactivity of the program counter during the corresponding clock cycle.

13. (New) The method of Claim 11, wherein said second number of packets is one.

14. (New) An apparatus for generating a timing trace stream that is associated with a target processor and includes logic signals respectively associated with clock cycles of the target processor, comprising:

an input for receiving said logic signals;

logic coupled to said input for providing a first control signal when any two of a preselected consecutive number of said logic signals have respectively different logic levels, and further for providing a second control signal when all of said preselected consecutive number of logic signals have a same logic level;

a first storage portion coupled to said input for storing each of said preselected consecutive number of logic signals, said first storage portion coupled to said logic and responsive to said first control signal for transferring the stored logic signals formatted within a first number of packets; and

a second storage portion coupled to said input for storing a first representation of said same logic level when all of said preselected consecutive number of logic signals have said same logic level, and said second storage portion further storing a second representation of a multiple of said preselected number, said second storage portion coupled to said logic and responsive to said second control signal for transferring said first and second representations formatted within a second number of said packets that is less than said first number of packets.

15. (New) The apparatus of Claim 14, wherein said second

number of packets is one.

16. (New) A system for transferring to a host processor information concerning the operation of a target processor, comprising:

a program counter trace stream generation unit configured to generate a trace stream that traces activity of a program counter in the target processor; and

a timing trace stream generation unit having first and second modes of operation, said first mode of operation generating timing trace streams for transmission to the host processor, said timing trace streams having logic signals respectively associated with clock cycles of the target processor, wherein a first logic level of the logic signal indicates an activity associated with the program counter during the associated clock cycle and a second logic level of the logic signal indicates an absence of activity associated with the program counter during the associated clock cycle, said second mode of operation generating a compressed timing trace output for transmission to the host processor instead of one of said timing trace streams if said one timing trace stream would have contained only logic signals having a same logic level, said compressed timing trace output including a first representation of said same logic level and a second representation of a number of said logic signals that said one trace timing stream would have contained, and said compressed timing trace output requiring less transmission bandwidth than said one timing trace stream.

17. (New) The system of Claim 16, wherein said timing trace streams are each formatted within a plurality of packets, and said compressed timing trace output is formatted within a single said packet.